REMARKS

Claims 1, 3-5, 7-9, 11-13, 15-18 are pending. Claims 1 and 13 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

It is respectfully requested that this Amendment be entered as it places the application in condition for allowance or at least in better form for appeal.

Applicant would like to thank Examiner Mondt and Examiner Flynn for the courtesies extended to the Applicant's representative during a November 1, 2002 personal interview. During the interview, Applicant's representative proposed amending claim 1 to include that the body region is exposed between the plurality of second semiconductor regions and indicated that this feature is not taught in the prior art of record. The Examiner agreed to consider such an Amendment.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 3-5, 7-9, 11-13, and 15-18 were rejected under 35 U.S.C. § 103(a) over Yamada (U.S. Patent No. 5,502,320) in view of Hshieh et al (U.S. Patent No. 5,986,304). Applicant respectfully traverses this rejection.

As amended, independent claim 1 recites, in part, that the body region is exposed between the plurality of second semiconductor regions and the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another. As discussed during the November 1, 2002 personal interview, neither Yamada or Hshieh discloses or teaches such a feature. Yamada, being directed to a memory device, discloses several layers on top of the substrate 1. Hshieh discloses that an N+ layer 115 is placed over the p-body region 120. Accordingly, no combination of Yamada and Hshieh teach or suggest that the body region is exposed between the plurality of second semiconductor regions, as recited in claim 1.

Independent claim 13 recites, in part, a process for producing a semiconductor device wherein the body region is exposed between the plurality of second semiconductor regions. Applicant submits that claim 13 is allowable for at least the same reasons presented above with regard to claim 1.

Claims 3-5, 7-9, 11,12, and 15-18 are believed allowable by virtue of their dependence from claims 1 and 13 for at least the reasons presented above with regard to

claims 1 and 13 in addition to their recitation of independent patentable subject matter. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Conclusion

Applicant appreciates that claims 17 and 18 have not been rejected under prior art. However, in view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 13 have been amended as follows:

1. (Twice Amended) A semiconductor device comprising:

a body region of a first conductivity type formed in a semiconductor substrate and having a major surface opposite to [the] a surface shared between the semiconductor substrate and the body region;

a plurality of trench gates extending through the body region;

a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates; and

a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth,

wherein the body region is exposed between the plurality of second semiconductor regions and the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

13. (Twice Amended) A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate, the body region having a major surface opposite to [the] a surface shared between the semiconductor substrate and the body region;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from said major surface of the body region, at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via films bordering and insulating the trench gates;

forming a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from said major surface of the body region that is less than the first depth; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions;

wherein the body region is exposed between the plurality of second semiconductor regions.

End of Appendix